FIG. 1

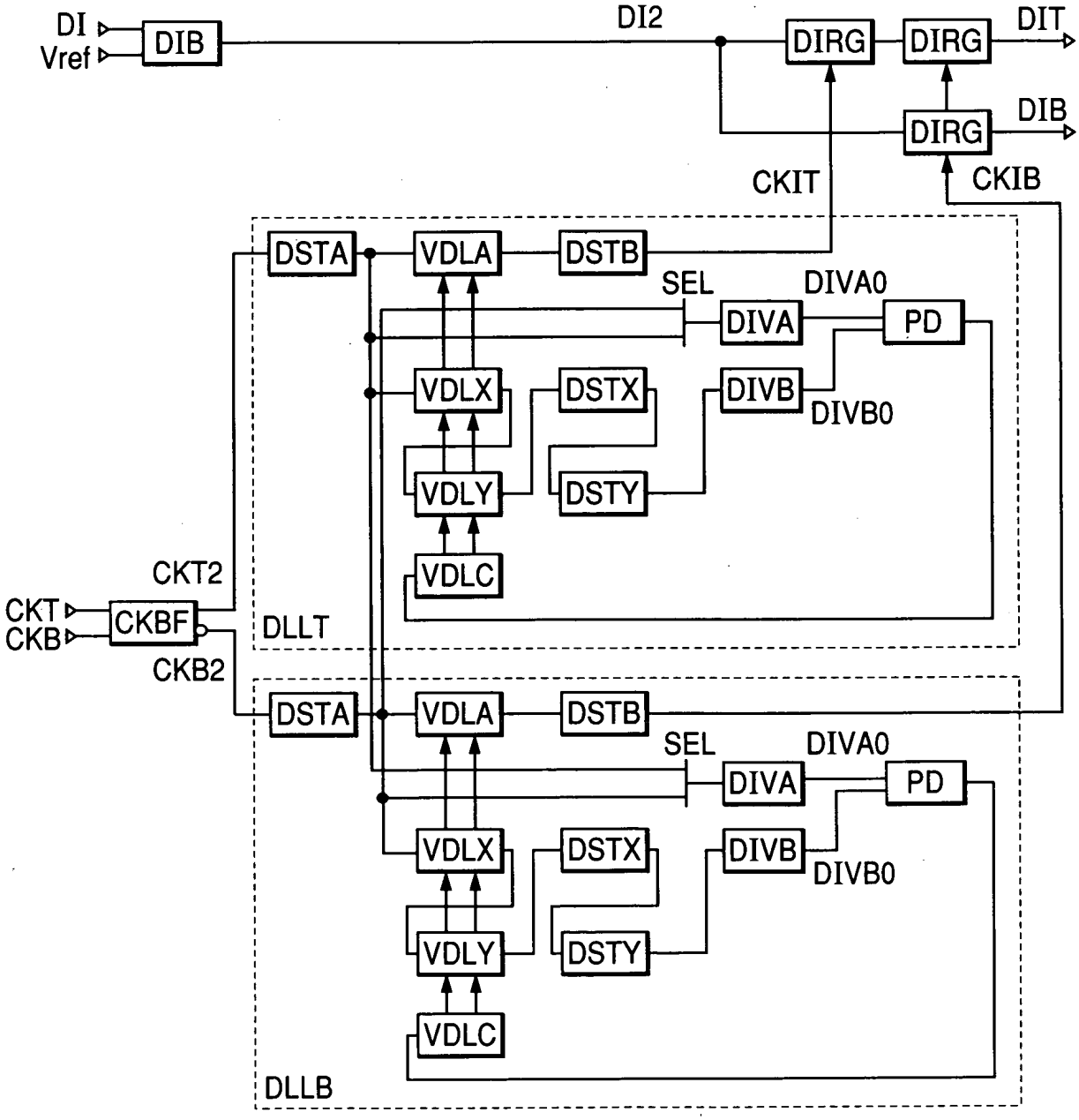

DI
Vref
DIB
DI2
DIRG
DIRG
DIT
DIRG
DIB
CKIT
CKIB
DSTA
VDLA
DSTB
SEL
DIVA0
DIVA
PD
VDLX
DSTX
DIVB
DIVB0
VDLY
DSTY
VDLC
CKT2
CKT
CKB
CKBF
CKB2
DLLT
DSTA
VDLA
DSTB
SEL
DIVA0
DIVA
PD
VDLX
DSTX
DIVB
DIVB0
VDLY
DSTY
VDLC
DLLB

FIG. 2

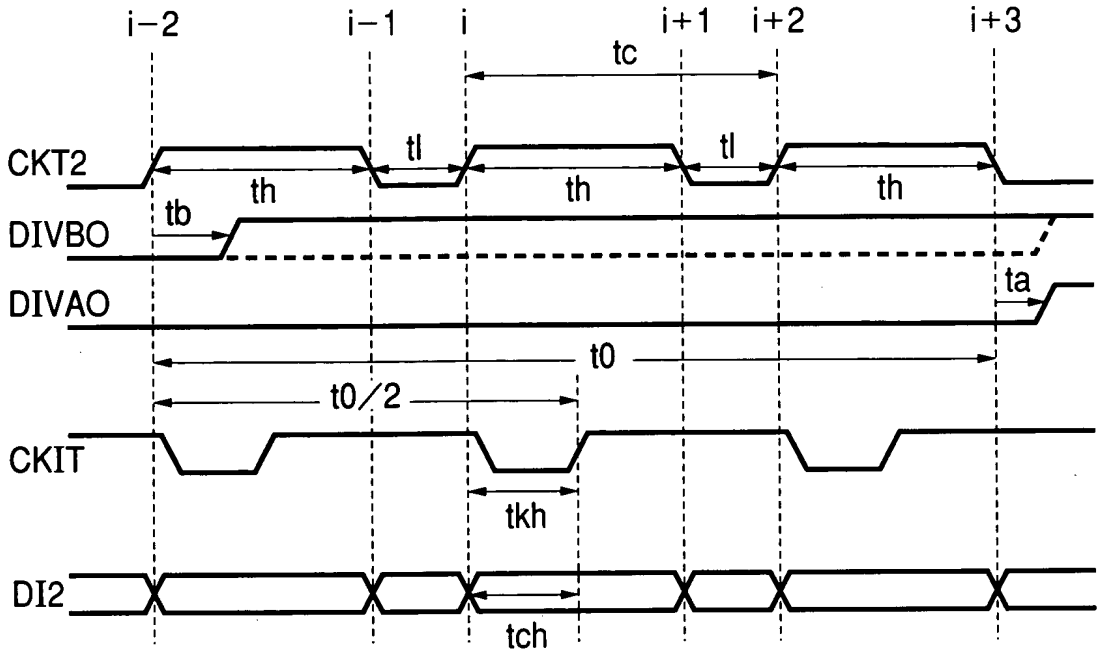

i−2
i−1
i
i+1
i+2
i+3
tc
CKT2
tl
tl
th
th
th
tb
DIVBO
ta
DIVAO
t0
t0/2
CKIT
tkh
DI2
tch

FIG. 3

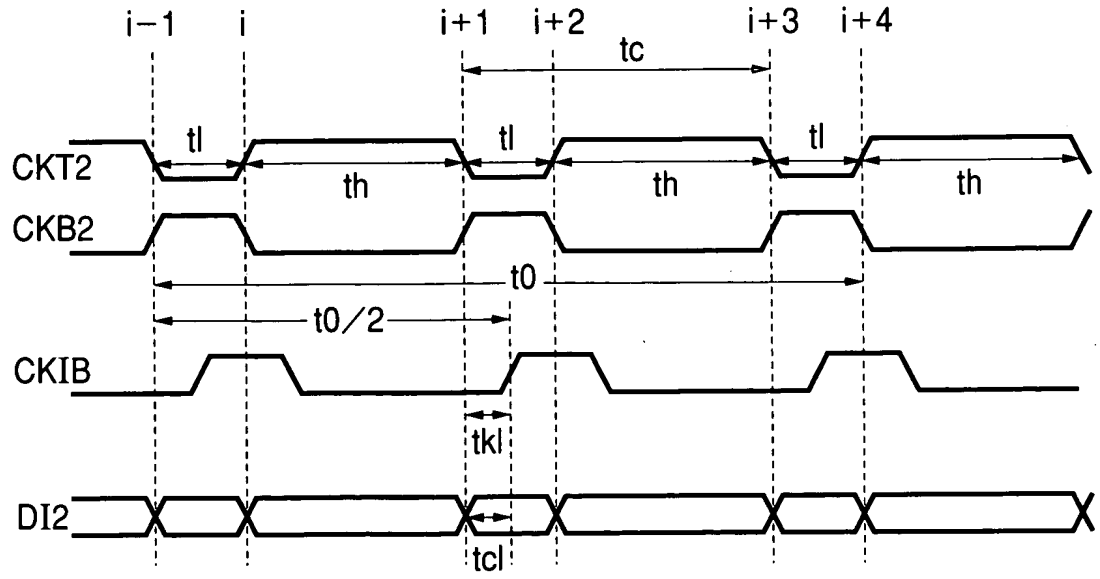

i−1
i
i+1
i+2
i+3
i+4
tc
tl
tl
tl
CKT2
th
th
th
CKB2
t0
t0/2
CKIB
tkl
DI2
tcl

FIG. 4

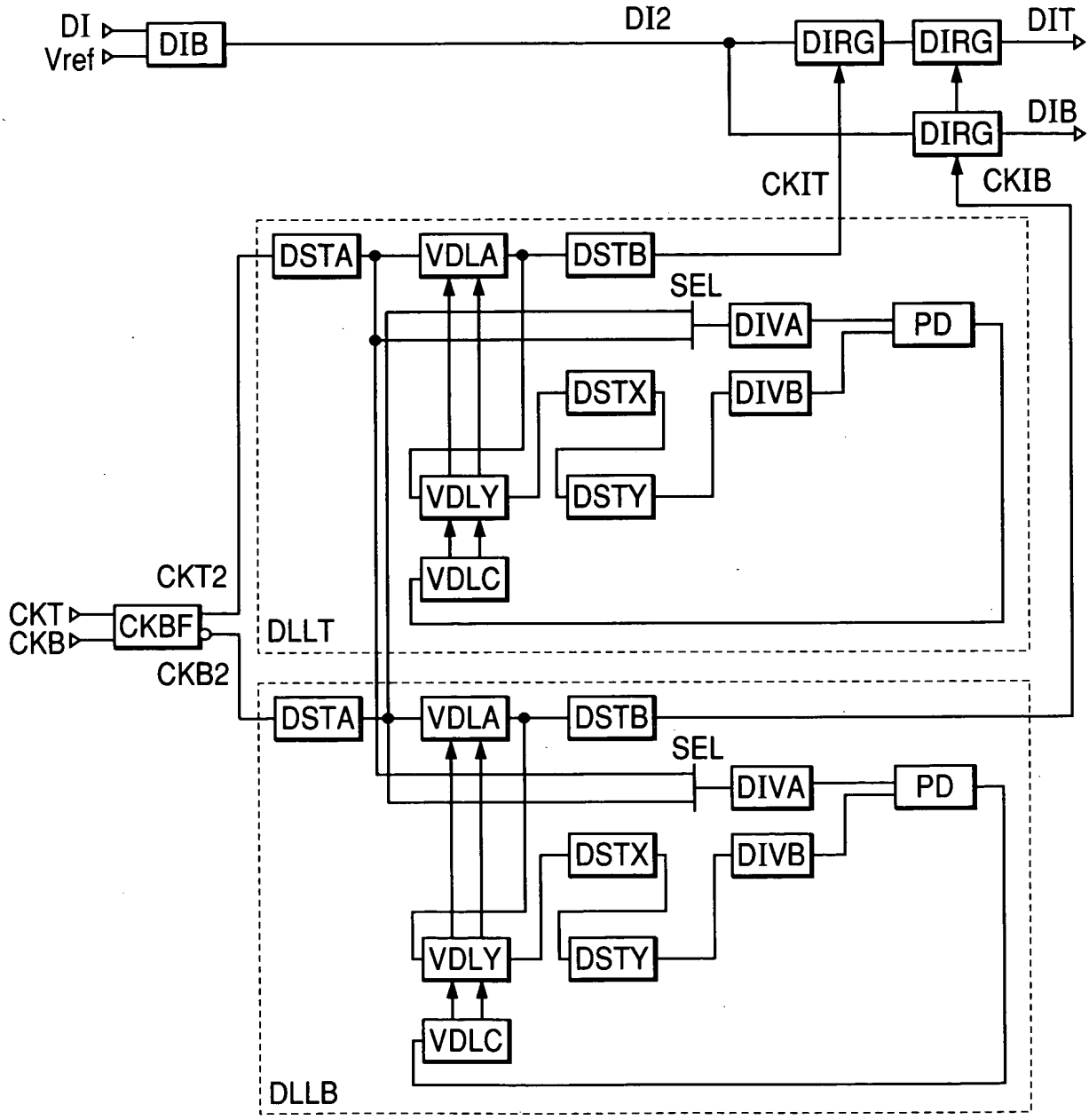

DI
Vref
DIB
DI2
DIRG
DIRG
DIT
DIRG
DIB
CKIT
CKIB
DSTA
VDLA
DSTB
SEL
DIVA
PD
DSTX
DIVB
VDLY
DSTY
VDLC
CKT2
CKT
CKB
CKBF
CKB2
DLLT
DSTA
VDLA
DSTB
SEL
DIVA
PD
DSTX
DIVB
VDLY
DSTY
VDLC
DLLB

FIG. 5

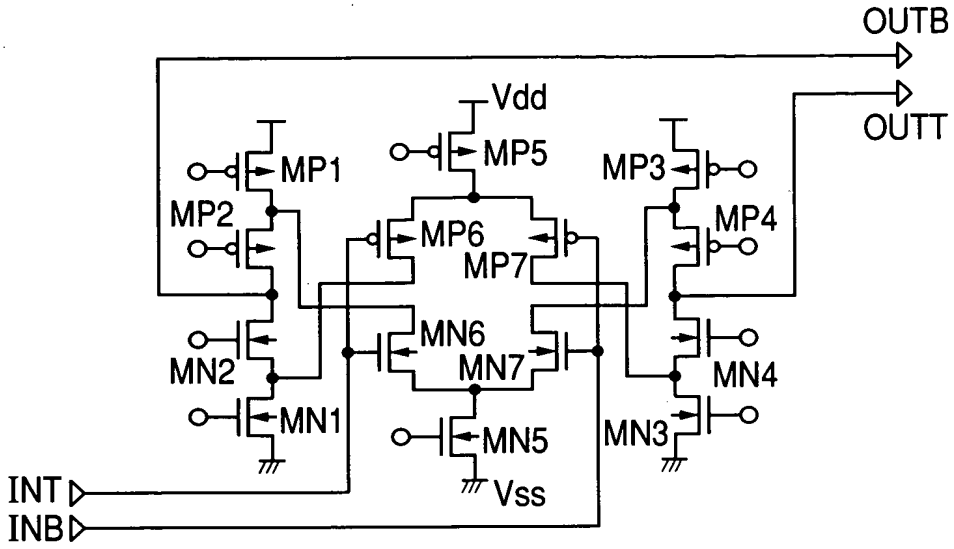
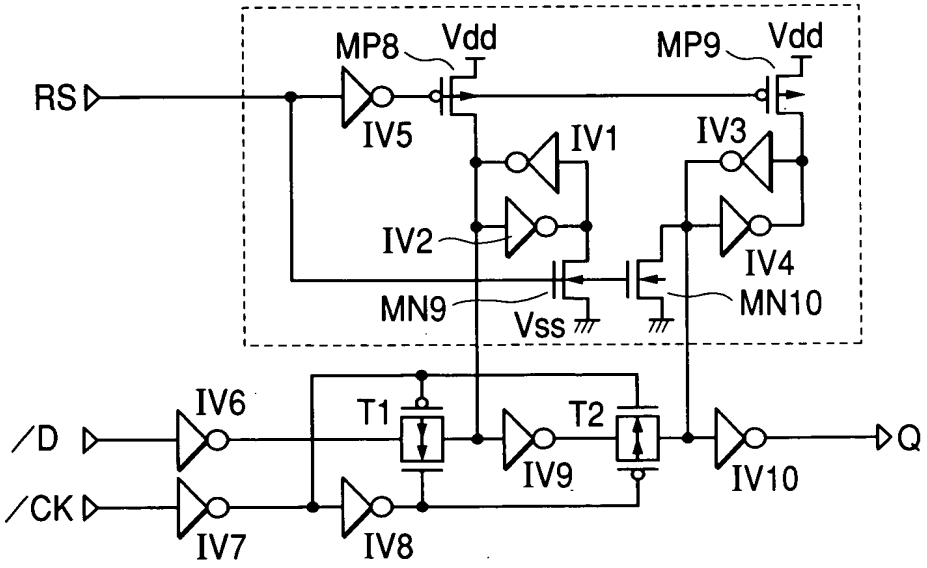

OUTB
OUTT
Vdd
MP1
MP5
MP3
MP2
MP6
MP4
MP7
MN6
MN2
MN7
MN4
MN1
MN5
MN3
Vss
INT
INB

FIG. 6


MP8
Vdd
MP9
Vdd
RS
IV5
IV1
IV3
IV2
IV4
MN9
Vss
MN10
IV6
T1
T2
/D
Q
IV9
IV10
/CK
IV7
IV8

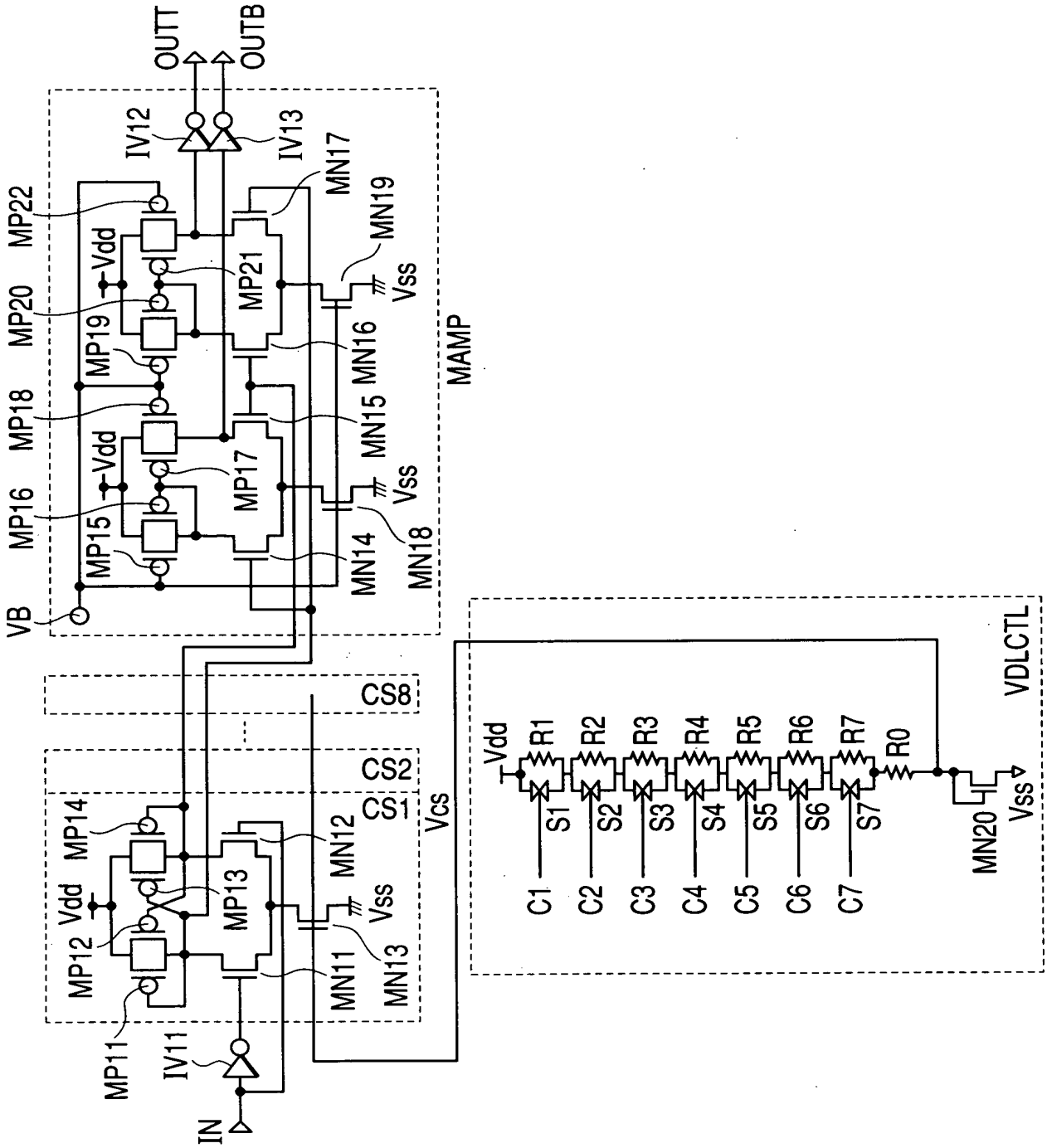

OUTT
OUTB
IV12
IV13
MP22
MP20
MP18
MP16
MP19
MP15
MP21
MP17
MN17
MN19
MN16
MN15
MN14
MN18
Vdd
Vss
VB
MAMP
CS8
CS2
CS1
Vcs
MP14
MP12
MP13
MN12
MN11
MN13
MP11
IV11
IN
Vdd
R1
R2
R3
R4
R5
R6
R7
R0
S1
S2
S3
S4
S5
S6
S7
C1
C2
C3
C4
C5
C6
C7
MN20
Vss
VDLCTL

FIG. 7

FIG. 8

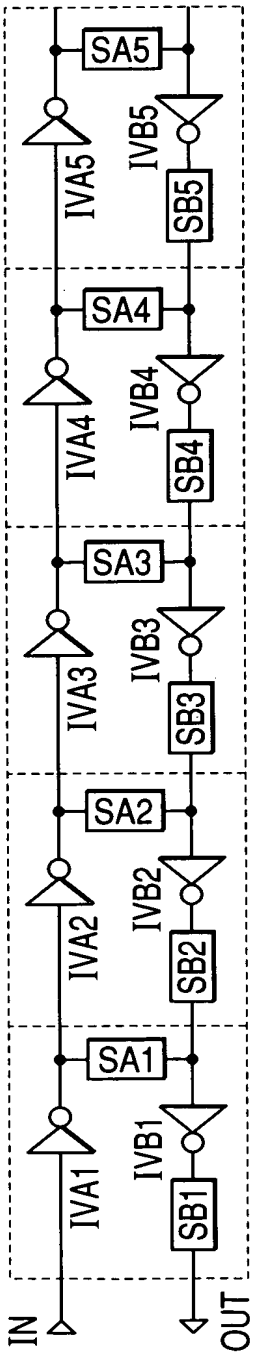

IN
OUT
IVA1
IVA2
IVA3
IVA4
IVA5
IVB1
IVB2
IVB3
IVB4
IVB5
SA1
SA2
SA3
SA4
SA5
SB1
SB2
SB3
SB4
SB5

FIG. 9

No.	SA1	SA2	SA3	SA4	SA5	SB1	SB2	SB3	SB4	SB5
1	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
2	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
3	OFF	OFF	ON	OFF	OFF	ON	ON	ON	OFF	OFF
4	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	OFF
5	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON

FIG. 10

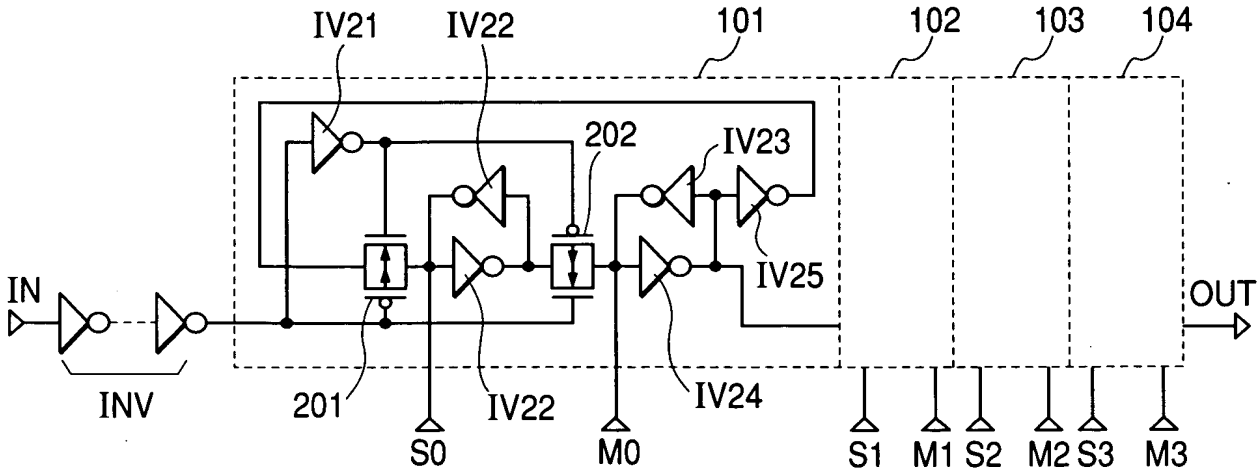


FIG. 11

"0" : LOW LEVEL
"1" : HIGH LEVEL
HZ : High-Z (HIGH IMPEDANCE)

No.	THE NUMBER OF INVS	S0	M0	S1	M1	S2	M2	S3	M3
1	EVEN NUMBER	HZ	1	HZ	1	HZ	1	HZ	1
2	ODD NUMBER	0	HZ	HZ	1	HZ	1	HZ	1
3	EVEN NUMBER	HZ	0	0	HZ	HZ	1	HZ	1
4	ODD NUMBER	1	HZ	0	HZ	HZ	1	HZ	1
5	EVEN NUMBER	HZ	1	HZ	0	0	HZ	HZ	1
6	ODD NUMBER	0	HZ	HZ	0	0	HZ	HZ	1
7	EVEN NUMBER	HZ	0	1	HZ	0	HZ	HZ	1
8	ODD NUMBER	1	HZ	1	HZ	0	HZ	HZ	1
9	EVEN NUMBER	HZ	1	HZ	1	HZ	0	0	HZ
10	ODD NUMBER	0	HZ	HZ	1	HZ	0	0	HZ
11	EVEN NUMBER	HZ	0	0	HZ	HZ	0	0	HZ
12	ODD NUMBER	1	HZ	0	HZ	HZ	0	0	HZ
13	EVEN NUMBER	HZ	1	HZ	0	1	HZ	0	HZ
14	ODD NUMBER	0	HZ	HZ	0	1	HZ	0	HZ
15	EVEN NUMBER	HZ	0	1	HZ	1	HZ	0	HZ
16	ODD NUMBER	1	HZ	1	HZ	1	HZ	0	HZ
17	EVEN NUMBER	HZ	1	HZ	1	HZ	1	HZ	0
18	ODD NUMBER	0	HZ	HZ	1	HZ	1	HZ	0
19	EVEN NUMBER	HZ	0	0	HZ	HZ	1	HZ	0
20	ODD NUMBER	1	HZ	0	HZ	HZ	1	HZ	0
21	EVEN NUMBER	HZ	1	HZ	0	0	HZ	HZ	0
22	ODD NUMBER	0	HZ	HZ	0	0	HZ	HZ	0
23	EVEN NUMBER	HZ	0	1	HZ	0	HZ	HZ	0
24	ODD NUMBER	1	HZ	1	HZ	0	HZ	HZ	0
25	EVEN NUMBER	HZ	1	HZ	1	HZ	0	1	HZ
26	ODD NUMBER	0	HZ	HZ	1	HZ	0	1	HZ
27	EVEN NUMBER	HZ	0	0	HZ	HZ	0	1	HZ
28	ODD NUMBER	1	HZ	0	HZ	HZ	0	1	HZ
29	EVEN NUMBER	HZ	1	HZ	0	1	HZ	1	HZ
30	ODD NUMBER	0	HZ	HZ	0	1	HZ	1	HZ
31	EVEN NUMBER	HZ	0	1	HZ	1	HZ	1	HZ
32	ODD NUMBER	1	HZ	1	HZ	1	HZ	1	HZ

FIG. 12

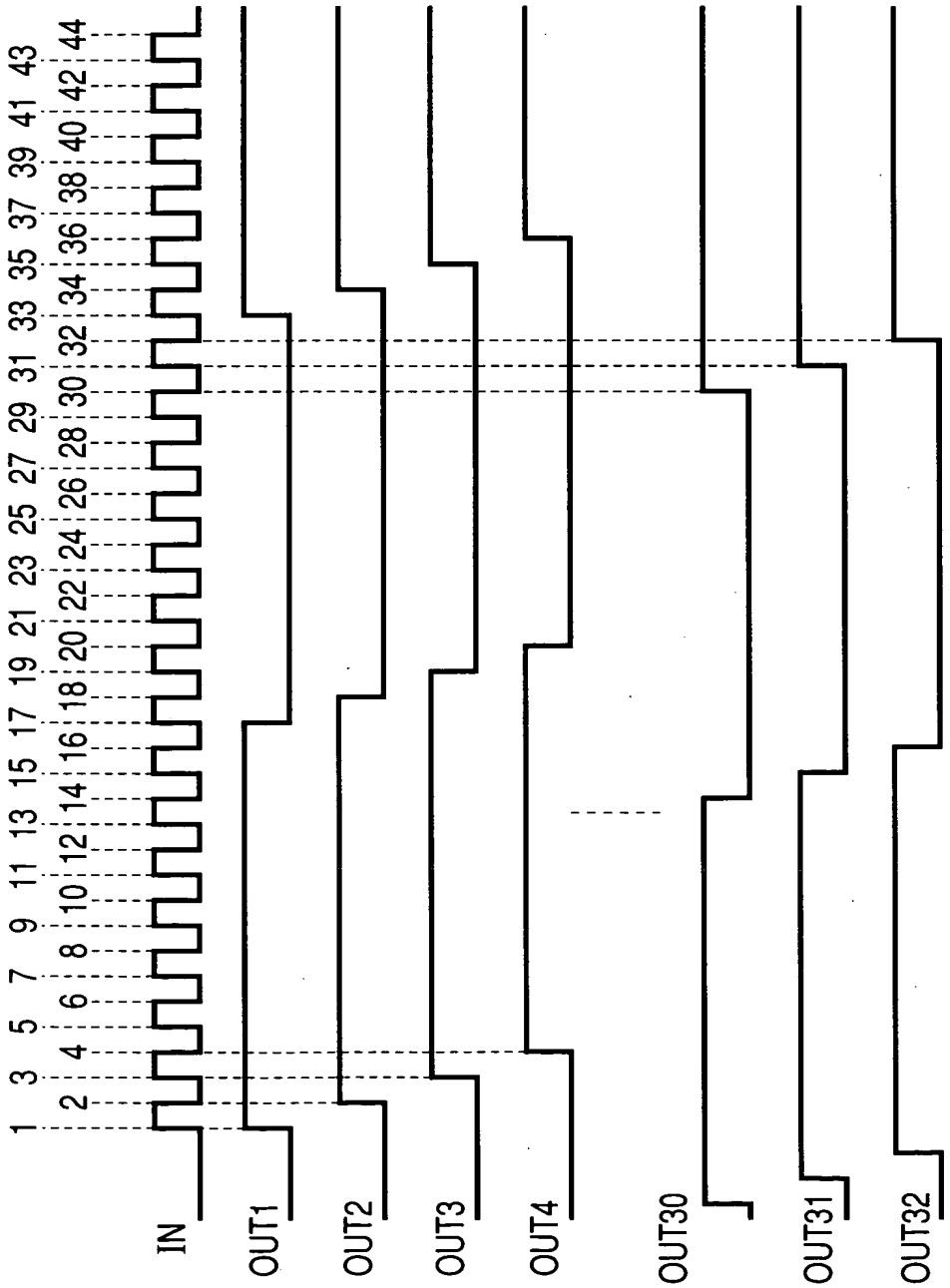

1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43
2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44
IN
OUT1
OUT2
OUT3
OUT4
OUT30
OUT31
OUT32

FIG. 13

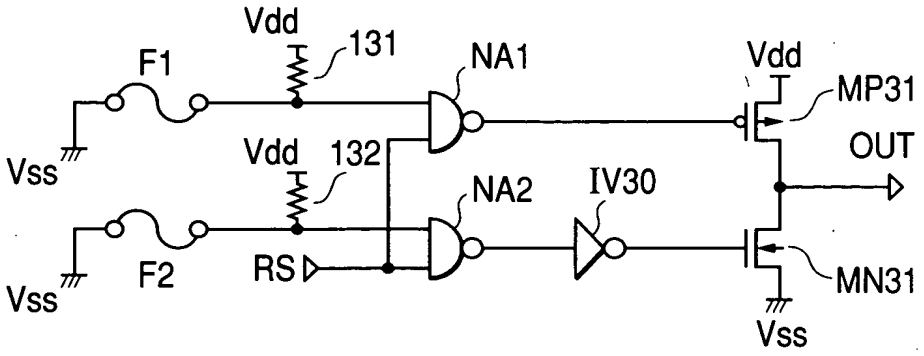
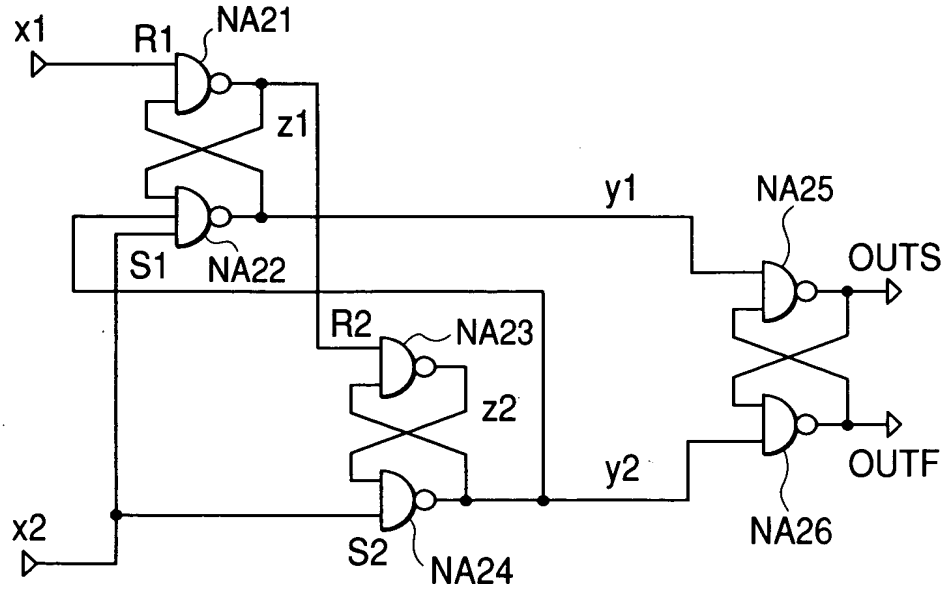

Vdd
131
F1
NA1
Vdd
MP31
Vss
Vdd
132
OUT
NA2
IV30
F2
RS
MN31
Vss
Vss

FIG. 14


x1
R1
NA21
z1
y1
NA25
S1
NA22
OUTS
R2
NA23
z2
OUTF
y2
x2
S2
NA24
NA26

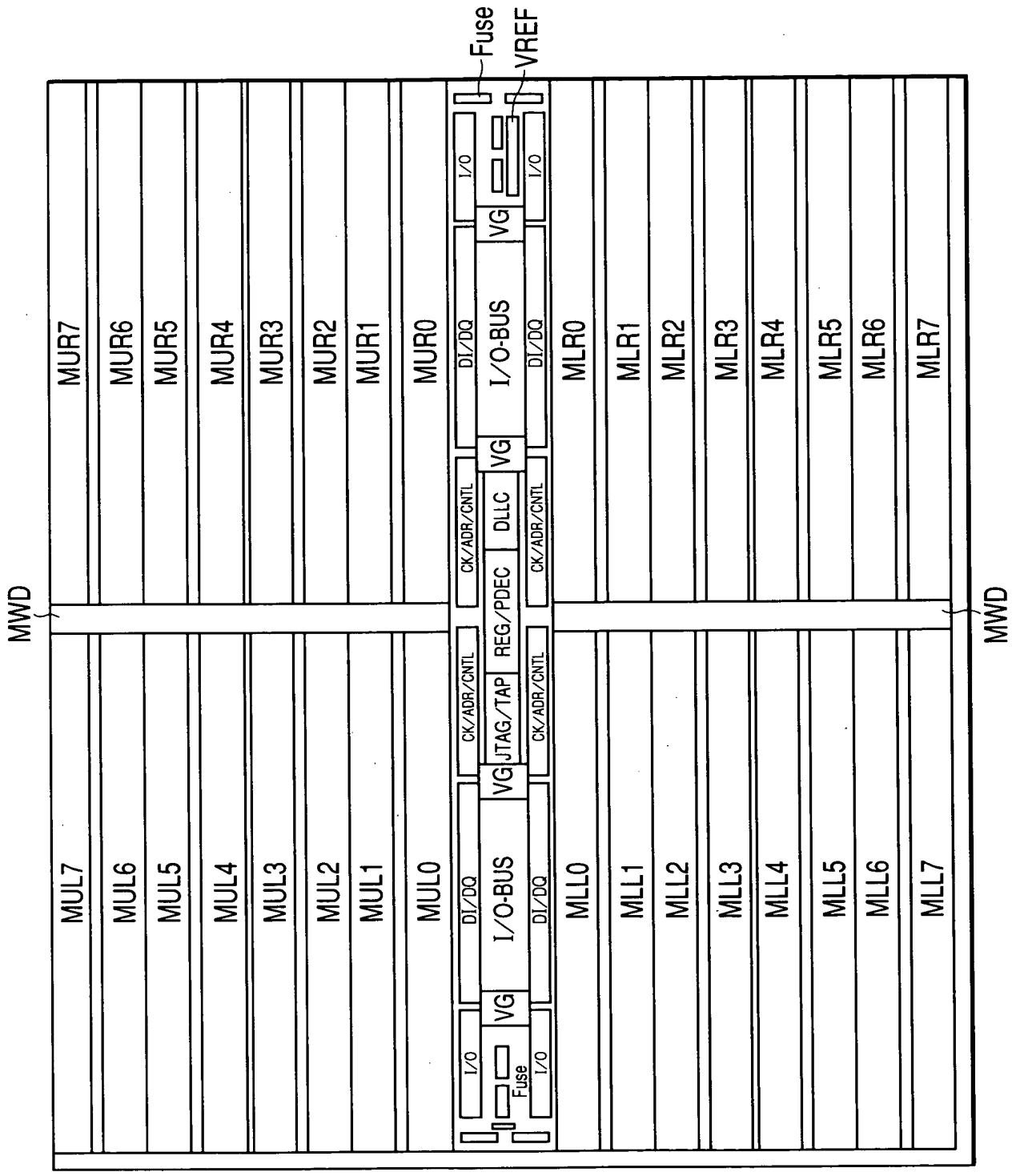

MUR7
MUR6
MUR5
MUR4
MUR3
MUR2
MUR1
MUR0
MUL7
MUL6
MUL5
MUL4
MUL3
MUL2
MUL1
MUL0
MLR0
MLR1
MLR2
MLR3
MLR4
MLR5
MLR6
MLR7
MLL0
MLL1
MLL2
MLL3
MLL4
MLL5
MLL6
MLL7
MWD
MWD
Fuse
VREF
I/O
VG
DI/DQ
I/O-BUS
CK/ADR/CNTL
JTAG/TAP
REG/PDEC
DLLC

FIG. 15

FIG. 16

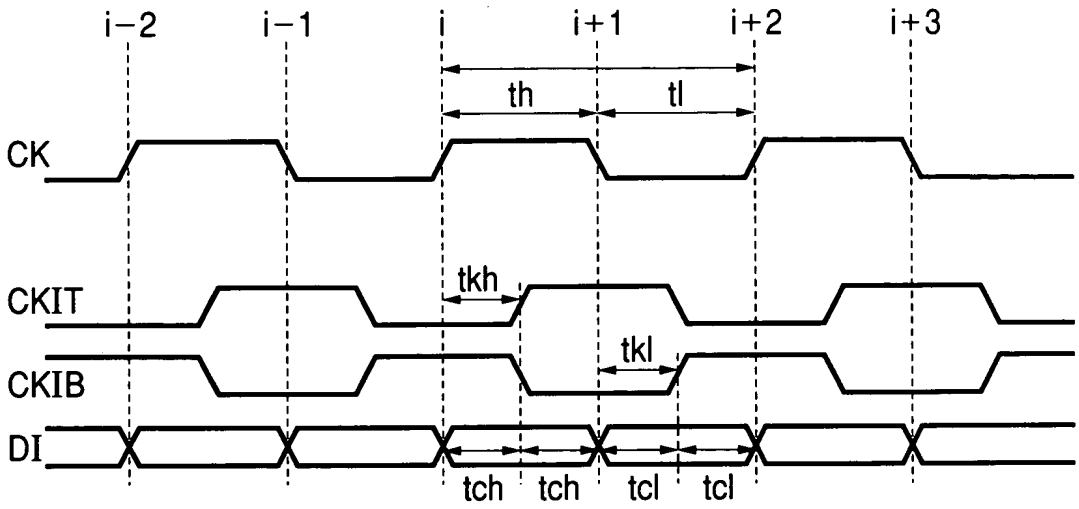
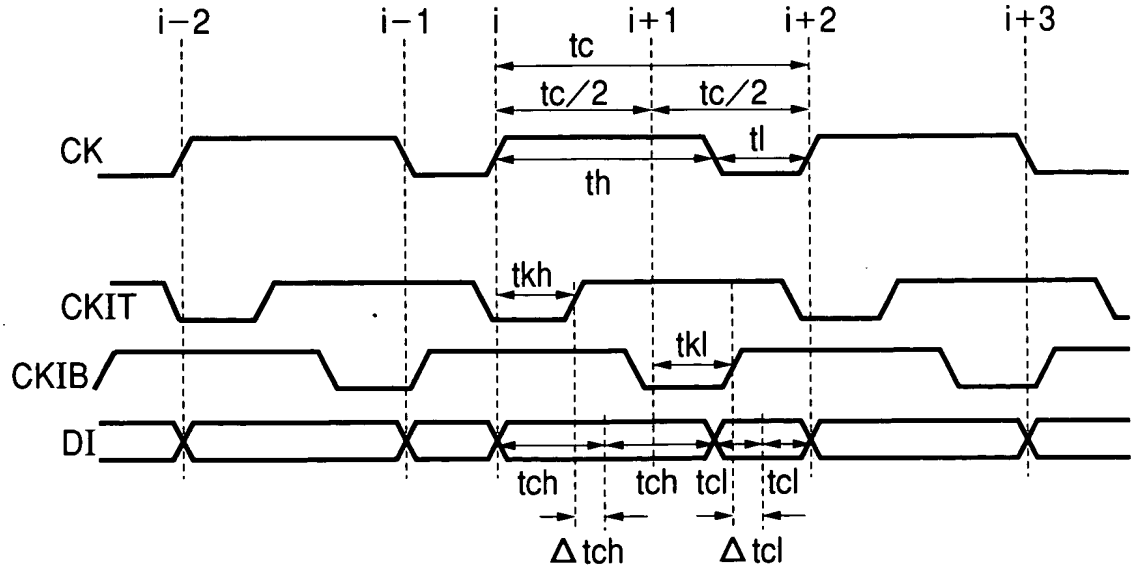

i−2
i−1
i
i+1
i+2
i+3
th
tl
CK
tkh
CKIT
tkl
CKIB
DI
tch
tch
tcl
tcl

FIG. 17


i−2
i−1
i
i+1
i+2
i+3
tc
tc/2
tc/2
tl
th
CK
tkh
CKIT
tkl
CKIB
DI
tch
tch
tcl
tcl
Δtch
Δtcl